CLAIMS

1. A method for monitoring fabrication of an integrated circuit (IC) on a semiconductor wafer, comprising:

generating a product design profile (PDP) using an electronic design automation (EDA) tool, the PDP comprising an indication of a site in at least one layer of the IC that is susceptible to a process fault;

fabricating the at least one layer of the IC on the wafer; and

applying a process monitoring tool to perform a measurement at the site in the at least one layer responsively to the PDP.

2. The method according to claim 1, wherein applying the process monitoring tool comprises measuring a dimension associated with one or more features of the IC at the site.

3. The method according to claim 1, wherein generating the PDP comprises making a determination that the site is critical to a performance rating of the IC, and selecting the site responsively to the determination.

4. The method according to claim 1, wherein generating the PDP comprises making a determination that the site is marginal with respect to a design rule of the IC, and selecting the site responsively to the determination.

5. The method according to claim 1, wherein generating the PDP comprises making a determination that the site is marginal with respect to a variation in a parameter of a process used in fabricating the IC, and selecting the site responsively to the determination.

6. The method according to claim 1, wherein generating the PDP comprises determining a mask error enhancement factor (MEEF) at the site, and selecting the site responsively to the MEEF.

7. The method according to claim 1, wherein generating the PDP comprises determining an optical proximity correction (OPC) to be applied at the site, and selecting the site responsively to the OPC.

8. The method according to claim 1, wherein generating the PDP comprises determining a density of structures in the IC at the site, and selecting the site responsively to the density.

9. The method according to claim 1, wherein the site comprises a location of a pair of matched circuit elements, and wherein applying the process monitoring tool comprises verifying that a critical characteristic of both the circuit elements in the pair is substantially identical.

10. The method according to claim 1, and comprising predicting a yield of the fabrication of the IC responsively to the PDP and to the measurement.

11. A method for monitoring fabrication of an integrated circuit (IC) on a semiconductor wafer, comprising:

generating a product design profile (PDP) using an electronic design automation (EDA) tool, the PDP comprising an identification of a region in at least one layer of the IC that is characterized by a periodic pattern;

fabricating the at least one layer of the IC on the wafer; and

applying a process monitoring tool to perform a measurement in the region of the at least one layer responsively to the periodic pattern.

12. The method according to claim 11, wherein generating the PDP comprises determining a pitch and a direction of the periodic pattern, and wherein applying the process monitoring tool comprises selecting a spatial filter responsively to the pitch and the direction, and performing optical inspection of the region using the spatial filter.

13. The method according to claim 11, wherein generating the PDP comprises determining a direction of the periodic pattern, and wherein applying the process monitoring tool comprises selecting a scan direction responsively to the direction of the periodic pattern, and inspecting the region while scanning over the region in the selected scan direction.

14. The method according to claim 11, wherein generating the PDP comprises determining an exact period of a repetitive feature in the periodic pattern, and wherein applying the process monitoring tool comprises capturing multiple images of the feature at locations on the wafer that are mutually spaced by the exact period, and comparing each of the images to another of the images or to a reference image.

15. The method according to claim 11, wherein applying the process monitoring tool comprises determining, responsively to the periodic pattern, a sensitivity setting to be applied by the process monitoring tool in detecting defects in the region, wherein different sensitivity settings are applied by the process

monitoring tool in different regions of the at least one layer.

16. A method for monitoring fabrication of an integrated circuit (IC) on a semiconductor wafer, comprising:

generating a product design profile (PDP) using an electronic design automation (EDA) tool, the PDP comprising an identification of a plurality of regions in at least one layer of the IC and a respective criticality parameter for each of the regions, indicative of a maximum tolerable defect size in each of the regions;

fabricating at least one layer of the IC on the wafer; and

applying a process monitoring tool to perform a measurement in one or more of the regions in at least one layer responsively to the respective criticality parameter.

17. The method according to claim 16, wherein applying the process monitoring tool comprises setting a defect detection threshold in each of the one or more of the regions responsively to the respective criticality parameter.

18. The method according to claim 16, wherein applying the process monitoring tool comprises selecting the one or more of the regions to inspect responsively to the respective criticality parameter.

19. The method according to claim 16, wherein applying the process monitoring tool comprises detecting a defect in one of the regions, and classifying the defect responsively to the criticality parameter.

20. A method for monitoring fabrication of an integrated circuit (IC) on a semiconductor wafer, comprising:

designing a layout of at least one layer of the IC using an electronic design automation (EDA) tool, at least one layer comprising a structure that is amenable to testing;

generating a product design profile (PDP) using the EDA tool, the PDP comprising information regarding the structure;

fabricating at least one layer of the IC on the wafer; and

applying a process monitoring tool to perform a measurement on the structure in at least one layer, responsively the information in the PDP.

21. The method according to claim 20, wherein the structure comprises a dedicated test structure.

22. The method according to claim 21, wherein the dedicated test structure is located in a non-die area of the wafer.

23. The method according to claim 20, wherein the structure comprises multiple elongate parallel conductors, and wherein applying the process monitoring tool comprises testing an electrical continuity of the conductors.

24. The method according to claim 23, wherein testing the electrical continuity comprises applying an electrical charge at a first end of at least some of the conductors, and measuring the electrical charge at a second end of the conductors.

25. The method according to claim 20, wherein the structure comprises one or more contact openings in at least one layer, and wherein applying the process monitoring tool comprises directing an electron beam to irradiate the one or more contact openings, and measuring a specimen current responsively to the electron beam.

26. Apparatus for producing an integrated circuit (IC) on a semiconductor wafer, comprising:

an electronic design automation (EDA) tool, which is adapted to generate a design of at least one layer of the IC and a product design profile (PDP), which comprises an indication of a site in at least one layer that is susceptible to a process fault;

a production tool, which is adapted to fabricate at least one layer of the IC on the wafer responsively to the design; and

a process monitoring tool, which is adapted to perform a measurement at the site in at least one layer responsively to the PDP.

27. The apparatus according to claim 26, wherein the process monitoring tool is adapted to measure a dimension associated with one or more features of the IC at the site.

28. The apparatus according to claim 26, wherein the indication is included in the PDP responsively to a determination that the site is critical to a performance rating of the IC.

29. The apparatus according to claim 26, wherein the indication is included in the PDP responsively to a determination that the site is marginal with respect to a design rule of the IC.

30. The apparatus according to claim 26, wherein the indication is included in the PDP responsively to a determination that the site is marginal with respect to a variation in a parameter of a process used in fabricating the IC.

31. The apparatus according to claim 26, wherein the EDA tool is adapted to determine a mask error enhancement factor (MEEF) at the site, and to select the site responsively to the MEEF.

32. The apparatus according to claim 26, wherein the EDA tool is adapted to determine an optical proximity correction (OPC) to be applied at the site, and to select the site responsively to the OPC.

33. The apparatus according to claim 26, wherein the EDA tool is adapted to select the site responsively to a density of structures in the IC at the site.

34. The apparatus according to claim 26, wherein the site comprises a location of a pair of matched circuit elements, and wherein the process monitoring tool is adapted to verify that a critical characteristic of both the circuit elements in the pair is substantially identical.

35. The apparatus according to claim 26, and comprising a computer processor, which is adapted to predict a yield of the fabrication of the IC responsively to the PDP and to the measurement.

36. Apparatus for producing an integrated circuit (IC) on a semiconductor wafer, comprising:

an electronic design automation (EDA) tool, which is adapted to generate a design of at least one layer of the

IC and a product design profile (PDP), which comprises an identification of a region in at least one layer of the IC that is characterized by a periodic pattern;

a production tool, which is adapted to fabricate at least one layer of the IC on the wafer responsively to the design; and

a process monitoring tool, which is adapted to perform a measurement in the region in at least one layer responsively to the periodic pattern.

37. The apparatus according to claim 36, wherein the PDP comprises an indication of a pitch and a direction of the periodic pattern, and wherein the process monitoring tool is adapted to perform optical inspection of the region using a spatial filter, wherein the spatial filter is selected responsively to the pitch and the direction indicated by the PDP.

38. The apparatus according to claim 36, wherein the PDP comprises an indication of a direction of the periodic pattern, and wherein the process monitoring tool is adapted to inspect the region while scanning over the region in the selected scan direction, wherein the scan direction is selected responsively to the direction of the periodic pattern indicated by the PDP.

39. The apparatus according to claim 36, wherein the PDP comprises an indication of an exact period of a repetitive feature in the periodic pattern, and wherein the process monitoring tool is adapted to capture multiple images of the feature at selected locations on the wafer and to compare each of the images to another of the images or to a reference image, wherein the selected locations are mutually spaced by the exact period.

40. The apparatus according to claim 36, wherein the process monitoring tool has a variable sensitivity setting, wherein different sensitivity settings are applied by the process monitoring tool for detecting defects in different regions of at least one layer, and wherein the sensitivity setting to be applied in the region is determined responsively to the periodic pattern.

41. Apparatus for producing an integrated circuit (IC) on a semiconductor wafer, comprising:

an electronic design automation (EDA) tool, which is adapted to generate a design of at least one layer of the IC and a product design profile (PDP), which comprises an identification of a plurality of regions in the at least one layer of the IC and a respective criticality parameter for each of the regions, indicative of a maximum tolerable defect size in each of the regions;

a production tool, which is adapted to fabricate at least one layer of the IC on the wafer responsively to the design; and

a process monitoring tool, which is adapted to perform a measurement in one or more of the regions responsively to the respective criticality parameter.

42. The apparatus according to claim 41, wherein a defect detection threshold of the process monitoring tool is set in each of the one or more of the regions responsively to the respective criticality parameter.

43. The apparatus according to claim 41, wherein the one or more of the regions to inspect are selected responsively to the respective criticality parameter.

44. The apparatus according to claim 41, wherein the process monitoring tool is adapted to detect a defect in one of the regions, and to classify the defect responsively to the criticality parameter.

45. Apparatus for producing an integrated circuit (IC) on a semiconductor wafer, comprising:

an electronic design automation (EDA) tool, which is adapted to generate a design of at least one layer of the IC, the layout comprising a structure that is amenable to testing, and which is further adapted to generate and a product design profile (PDP), which comprises information regarding the structure;

a production tool, which is adapted to fabricate at least one layer of the IC on the wafer responsively to the design; and

a process monitoring tool, which is adapted to perform a measurement on the structure, responsively the information in the PDP.

46. The apparatus according to claim 45, wherein the structure comprises a dedicated test structure.

47. The apparatus according to claim 46, wherein the dedicated test structure is located in a non-die area of the wafer.

48. The apparatus according to claim 45, wherein the structure comprises multiple elongate parallel conductors, and wherein the process monitoring tool is adapted to test an electrical continuity of the conductors.

49. The apparatus according to claim 48, wherein the process monitoring tool is adapted to test the electrical

continuity by applying an electrical charge at a first end of at least some of the conductors, and measuring the electrical charge at a second end of the conductors.

50. The apparatus according to claim 45, wherein the structure comprises one or more contact openings in at least one layer, and wherein the process monitoring tool is adapted to direct an electron beam to irradiate the one or more contact openings, and to measure a specimen current responsively to the electron beam.

51. A computer software product for use in producing an integrated circuit (IC) on a semiconductor wafer, the product comprising a computer-readable medium in which program instructions are stored, the instructions comprising at least one of an electronic design automation (EDA) program component and a process monitoring program component,

wherein the EDA program component, when read by a computerized EDA tool, causes the EDA tool to generate a design of at least one layer of the IC and a product design profile (PDP), which comprises an indication of a site in at least one layer that is susceptible to a process fault, and

wherein the process monitoring program component, when read by a computerized process monitoring tool after fabrication of at least one layer of the IC on the wafer responsively to the design, causes the process monitoring tool to perform a measurement at the site in at least one layer responsively to the PDP.

52. The product according to claim 51, wherein the process monitoring program component causes the process

monitoring tool to measure a dimension associated with one or more features of the IC at the site.

53. The product according to claim 51, wherein the EDA program component causes the EDA tool to make a determination that the site is critical to a performance rating of the IC, and to include the site in the PDP responsively to the determination.

54. The product according to claim 51, wherein the EDA program component causes the EDA tool to make a determination that the site is marginal with respect to a design rule of the IC, and to include the site in the PDP responsively to the determination.

55. The product according to claim 51, wherein the EDA program component causes the EDA tool to make a determination that the site is marginal with respect to a variation in a parameter of a process used in fabricating the IC, and to include the site in the PDP responsively to the determination.

56. The product according to claim 51, wherein the EDA program component causes the EDA tool to determine a mask error enhancement factor (MEEF) at the site, and to select the site responsively to the MEEF.

57. The product according to claim 51, wherein the EDA program causes the EDA tool to determine an optical proximity correction (OPC) to be applied at the site, and to select the site responsively to the OPC.

58. The product according to claim 51, wherein the EDA program causes the EDA tool to select the site responsively to a density of structures in the IC at the site.

59. The product according to claim 51, wherein the site comprises a location of a pair of matched circuit elements, and wherein the process monitoring program component causes the process monitoring tool to verify that a critical characteristic of both the circuit elements in the pair is substantially identical.

60. The product according to claim 51, wherein the process monitoring program component further causes the process monitoring tool to predict a yield of the fabrication of the IC responsively to the PDP and to the measurement.

61. A computer software product for use in producing an integrated circuit (IC) on a semiconductor wafer, the product comprising a computer-readable medium in which program instructions are stored, the instructions comprising at least one of an electronic design automation (EDA) program component and a process monitoring program component,

wherein the EDA program component, when read by a computerized EDA tool, causes the EDA tool to generate a design of at least one layer of the IC and a product design profile (PDP), which comprises an identification of a region in the at least one layer of the IC that is characterized by a periodic pattern, and

wherein the process monitoring program component, when read by a computerized process monitoring tool after fabrication of at least one layer of the IC on the wafer responsively to the design, causes the process monitoring tool to perform a measurement in the region in at least one layer responsively to the periodic pattern.

62. The product according to claim 61, wherein the EDA program component causes the EDA tool to include in the PDP an indication of a pitch and a direction of the periodic pattern, so that the process monitoring tool performs optical inspection of the region using a spatial filter that is selected responsively to the pitch and the direction indicated by the PDP.

63. The product according to claim 61, wherein the EDA program component causes the EDA tool to include in the PDP an indication of a direction of the periodic pattern, and wherein the process monitoring program component causes the process monitoring tool to inspect the region while scanning over the region in the selected scan direction, wherein the scan direction is selected responsively to the direction of the periodic pattern indicated by the PDP.

64. The product according to claim 61, wherein the EDA program component causes the EDA tool to include in the PDP an indication of an exact period of a repetitive feature in the periodic pattern, and wherein the process monitoring program component causes the process monitoring tool to capture multiple images of the feature at selected locations on the wafer and to compare each of the images to another of the images or to a reference image, wherein the selected locations are mutually spaced by the exact period.

65. The product according to claim 61, wherein the process monitoring tool has a variable sensitivity setting, and wherein the process monitoring program component causes the process monitoring tool to apply different sensitivity settings in detecting defects in

different regions of at least one layer, wherein the sensitivity setting to be applied in the region is determined responsively to the periodic pattern.

66. A computer software product for use in producing an integrated circuit (IC) on a semiconductor wafer, the product comprising a computer-readable medium in which program instructions are stored, the instructions comprising at least one of an electronic design automation (EDA) program component and a process monitoring program component,

wherein the EDA program component, when read by a computerized EDA tool, causes the EDA tool to generate a design of at least one layer of the IC and a product design profile (PDP), which comprises an identification of a plurality of regions in the at least one layer of the IC and a respective criticality parameter for each of the regions, indicative of a maximum tolerable defect size in each of the regions, and

wherein the process monitoring program component, when read by a computerized process monitoring tool after fabrication of at least one layer of the IC on the wafer responsively to the design, causes the process monitoring tool to perform a measurement in one or more of the regions responsively to the respective criticality parameter.

67. The product according to claim 66, wherein the process monitoring program component causes a defect detection threshold of the process monitoring tool to be set in each of the one or more of the regions responsively to the respective criticality parameter.

68. The product according to claim 66, wherein the one or more of the regions to inspect are selected responsively to the respective criticality parameter.

69. The product according to claim 66, wherein the process monitoring program component causes the process monitoring tool to detect a defect in one of the regions, and to classify the defect responsively to the criticality parameter.

70. A computer software product for use in producing an integrated circuit (IC) on a semiconductor wafer, the product comprising a computer-readable medium in which program instructions are stored, the instructions comprising at least one of an electronic design automation (EDA) program component and a process monitoring program component,

wherein the EDA program component, when read by a computerized EDA tool, causes the EDA tool to generate a design of at least one layer of the IC, the layout comprising a structure that is amenable to testing, and a product design profile (PDP), which comprises information regarding the structure, and

wherein the process monitoring program component, when read by a computerized process monitoring tool after fabrication of at least one layer of the IC on the wafer responsively to the design, causes the process monitoring tool to perform a measurement on the structure, responsively the information in the PDP.

71. The product according to claim 70, wherein the structure comprises a dedicated test structure.

72. The product according to claim 71, wherein the dedicated test structure is located in a non-die area of the wafer.

73. The product according to claim 70, wherein the structure comprises multiple elongate parallel conductors, and wherein the process monitoring program component causes the process monitoring tool to test an electrical continuity of the conductors.

74. The product according to claim 73, wherein the process monitoring tool causes the process monitoring tool to test the electrical continuity by applying an electrical charge at a first end of at least some of the conductors, and measuring the electrical charge at a second end of the conductors.

75. The product according to claim 70, wherein the structure comprises one or more contact openings in at least one layer, and wherein the process monitoring program component causes the process monitoring tool to direct an electron beam to irradiate the one or more contact openings, and to measure a specimen current responsively to the electron beam.

76. Apparatus for monitoring production of an integrated circuit (IC) on a semiconductor wafer, following fabrication of at least one layer of the IC on the wafer responsively to a design and a product design profile (PDP) generated by an electronic design automation (EDA) tool, the PDP including an indication of a site in at least one layer that is susceptible to a process fault, the apparatus comprising:

a process monitoring tool, which is adapted to perform a measurement at the site in at least one layer responsively to the PDP.

77. The apparatus according to claim 76, wherein the process monitoring tool is adapted to measure a dimension associated with one or more features of the IC at the site.

78. The apparatus according to claim 76, wherein the indication in the PDP indicates that the site is critical to a performance rating of the IC.

79. The apparatus according to claim 76, wherein the indication in the PDP indicates that the site is marginal with respect to a design rule of the IC.

80. The apparatus according to claim 76, wherein the indication in the PDP indicates that the site is marginal with respect to a variation in a parameter of a process used in fabricating the IC.

81. The apparatus according to claim 76, wherein the site comprises a location of a pair of matched circuit elements, and wherein the process monitoring tool is adapted to verify that a critical characteristic of both the circuit elements in the pair is substantially identical.

82. The apparatus according to claim 76, and comprising a computer processor, which is adapted to predict a yield of the fabrication of the IC responsively to the PDP and to the measurement.